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Highly Programmable Test Pattern Generation with Optimized DFT Architecture for VLSI Testing

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Abstract: *Many attempts have been carried out to overcome the bottleneck of test data bandwidth between the tester and the chip in the concept of combining BIST and test data compression. In this paper we present a new test data-compression scheme that is a hybrid approach between external testing and Built-In Self-Test (BIST). The proposed approach is based on Low-Power (LP) programmable generator capable of producing pseudorandom test patterns with desired toggling levels and enhanced fault coverage gradient compared with the best-to-date Built-In Self-Test (BIST) based pseudorandom test pattern generators. The same technique is extended to deterministically guide the ring generator toward predefined test sequences with improved fault-coverage for test cube based decompression. Furthermore, the proposed LP test compression method efficiency is proved by compare it with existing methods that allows the accurate test power envelope during testing mode. The efficiency of BIST in power reduction through transition control is also proved with benchmark circuits.*

I. INTRODUCTION

In the production of integrated circuits, testing is done to identify defective chips [1]. This is very important for shipping high quality products. Testing is also done to diagnose the reason for a chip failure in order to improve the manufacturing process. In system maintenance, testing is done to identify parts that need to be replaced in order to repair a system. Testing a digital circuit involves applying an appropriate set of input patterns to the circuit and checking for the correct outputs. The conventional approach is to use an external tester to perform the test. However, built-in self-test (BIST) techniques [2] have been developed in which some of the tester functions are incorporated on the chip enabling the chip to test itself. BIST provides a number of well-known advantages. It eliminates the need for expensive testers. It provides fast location of failed units in a system because the chips can test themselves concurrently. Fig1 is a block diagram showing the architecture for BIST.

The circuit that is being tested is called the circuit-under-test (CUT)[2]. There is a test pattern generator which applies test patterns to the CUT and an output response analyzer which checks the outputs. The test pattern generator must generate a set of test patterns that provides a high fault coverage in order to thoroughly test the CUT. Pseudo-random testing is an attractive approach for BIST. A linear feedback shift register (LFSR) can be used to apply pseudo-random patterns to the CUT. An LFSR has a simple structure requiring small area overhead. Moreover, an LFSR can also be used as an output response analyzer thereby serving a dual purpose. BIST techniques such as circular BIST [5], and BILBO registers [3] make use of this advantage to reduce overhead.

BIST is insufficient, then there are two solutions. One is to modify the circuit-under-test to make it random pattern testable, and the other is to modify the test pattern generator so that it generates patterns that detect the r.p.r. faults. Innovative techniques for both of these approaches are described in this dissertation. These techniques enable automated design of pseudo-random BIST implementations that satisfy fault coverage requirements while minimizing area and performance overhead. These techniques have been incorporated in the TOPS [4] (Totally Optimized Synthesis-for-test) tool being developed at the Center for Reliable Computing.

If the fault coverage for pseudo-random The standard PRPG method has been used as the test pattern generator for the BIST. A PRNG is a shift register where the input is a linear function of two or more bits (taps). It consists of D flip-flops and linear exclusive-OR (XOR) gates. It is considered an external exclusive-OR PRPG [3] as the feedback network of the XOR gates feeds externally from X0 to Xn-1. One of the two main parts of an LFSR is the shift register. A shift register is used to shift its contents into adjacent positions within the register or, in the case of the position on the end, output of the register.The BIST hardware architecture in more detail. In this project, the BIST module in the IOP is developed based on the architecture. Basically, a design with embedded BIST architecture consists of a test controller, hardware pattern generator, input multiplexer, circuit

under test (CUT) which in this project is the IOP and output response compactor. Optionally, a design with BIST capability may includes also the comparator and Read-Only-Memory (ROM) [3]

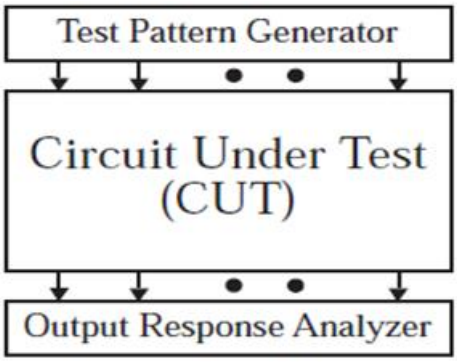


Fig.1 Block Diagram for BIST

II. RELATED WORK

Increasing the correlation among adjacent test stimulus bits can significantly reduce shift power consumption. However, it often causes test coverage loss when applying it to reduce the shift power consumption in logic BIST. In this paper, a new adaptive low shift power random test pattern generator (ALP-RTPG) [2] is presented to improve the tradeoff between test coverage loss and shift power reduction in logic BIST. This is achieved by applying the information derived from test responses to dynamically adjust the correlation among adjacent test stimulus bits. When comparing with an existing method, called LT-RTPG [3], experimental results for industrial designs show that the proposed method can significantly reduce the test coverage loss while still achieving dramatic shift power reduction. A modified linear feedback shift register (LFSR) [4] is presented that reduces the number of transitions at the inputs of the circuit-under test by 25% using a bit-swapping technique. Experimental results on ISCAS'85 and 89 benchmark circuits' show up to 45% power reduction during test. They also show that the proposed design can be combined with the techniques to achieve a very substantial power reduction of up to 63%. No test points or any medications' are made to the function logic. The paper describes the proposed hybrid BIST architecture as well as two different ways of storing the weight sets, which are an integral part of this scheme. It relies on a new type of test pattern generator which resembles a pro-grammable Johnson counter [2] and is called folding counter. Both the theoretical background and practica algorithms are presented to characterize a set of deterministic test cubes by a reasonably small number of seeds for a folding counter. Combined with classical approaches for test width compression and with pseudo-random pattern generation these new techniques provide an efficient and flexible solution for scan-based BIST [5]. Experimental results show that the proposed scheme outperforms previously published approaches based on the reseeding of LFSRs or Johnson counters.

III. DESIGN OF PRESTO GENERATOR

A digital system is tested and diagnosed during its lifetime on numerous occasions. It is very critical to have quick and very high fault coverage testing. One common and widely used in semiconductor industry for IC chip testing is to ensure this is to specify test as one of the system functions and thus becomes self-test. A system designed without an integrated test strategy which covering all levels from the entire system to components is being described as chip-wise and system-foolish. A proper designed Built-In-Self-Test (BIST) is able to offset the cost of added test hardware while at the same time ensuring the reliability, testability and reduce maintenance cost [5].The basic idea of BIST, in its most simple form, is to design a circuit so that the circuit can test itself and determine whether it is "good" or "bad" (fault-free or faulty, respectively). This typically requires additional circuitry whose functionality must be capable of generating test patterns as well as providing a mechanism to determine if the output responses of the circuit under test (CUT) to the test patterns correspond to that of a fault-free circuit . In all the cases test-per-clock and the test-per-scan schemes are required . Pseudorandom built-in self test (BIST) generators have been widely utilized to test integrated circuits and systems. The arsenal of pseudorandom generators includes, among others, linear feedback shift registers (LFSRs), cellular automata, and accumulators driven by a constant value. For circuits with hard-to-detect faults, a large number of random patterns have to be generated before high fault coverage is achieved. In many case we used a clock gating technique where two non overlapping clocks control the odd and even scan cells of the scan chain so that the shift power dissipation is reduced by a factor of two.

The ring generator can generate a single-input change (SIC) [3] sequence which can effectively reduce test power. The third approach aims to reduce the dynamic power dissipation during scan shift through gating of the outputs of a portion of the scan cells. Several low-power approaches have also been proposed for scan-based BIST. It will modifies scan-path structures, and lets the CUT inputs remain unchanged during a shift operation. Using multiple scan chains with many scan enable (SE) inputs [4] to activate one scan chain at a time, the TPG proposed in can reduce average power consumption during scan-based tests and the peak power in the CUT[4].In a pseudorandom BIST scheme was proposed to reduce switching activities in scan chains. However, modules containing hard-to-detect faults still require extra test hardware either by inserting test points into the mission logic or by storing additional deterministic test patterns. In order to overcome this problem, an accumulator-based weighted pattern generation scheme was proposed. The scheme generates test patterns having one of three weights, namely 0, 1, and 0.5 therefore it can be utilized to drastically reduce the test application time in accumulator- based test pattern generation. However, the scheme proposed in possesses three major drawbacks More precisely it does not impose any requirements about the design of the adder (i.e., it can be implemented using any adder design) it does not require any modification of the adder and hence does not affect the operating speed of the adder. Furthermore, the proposed scheme compares favorably to the scheme proposed and in terms of the required hardware overhead.

In this paper, we propose a PRPG for LP BIST applications. The generator primarily aims at reducing the switching activity during scan loading due to its preselected toggling (PRESTO) levels.

1) Minimum transitions: In the proposed pattern, each generated vector applied to each PRPG output, which can minimize the input transition and reduce test power.

2) Uniqueness of patterns: The proposed sequence does not contain any repeated patterns, and the number of distinct patterns in a sequence can meet the requirement of the target fault coverage for the CUT.

3) Uniform distribution of patterns: The conventional algorithms of modifying the test vectors generated by the LFSR use extra hardware to get more correlated test vectors with a low number of transitions. However, they may reduce the randomness in the patterns, which may result in lower fault coverage and higher test time.

4) Low hardware overhead consumed by extra TPGs[3]: The linear relations are selected with consecutive vectors or within a pattern, which has the benefit of generating a sequence with a sequential de-compressor[5]. Hence, the proposed TPG can be easily implemented by hardware.An n-bit PRPG [5] connected with a phase shifter feeding scan chains forms a kernel of the generator producing the actual pseudorandom test patterns. A linear feedback shift register or a ring generator can implement a PRPG. More importantly, however, n hold latches are placed between the PRPG and the phase shifter. Each hold latch is individually controlled via a corresponding stage of an n-bit toggle control register. As long as its enable input is asserted, the given latch is transparent for data going from the PRPG to the phase shifter, and it is said to be in the toggle mode. When the latch is disabled, it captures and saves, for a number of clock cycles, the corresponding bit of PRPG, thus feeding the phase shifter (and possibly some scan chains) with a constant value. It is now in the hold mode. It is worth noting that each phase shifter output is obtained by XOR-ing outputs of three different hold latches. Therefore, every scan chain remains in a low-power mode provided only disabled hold latches drive the corresponding phase shifter output[4]

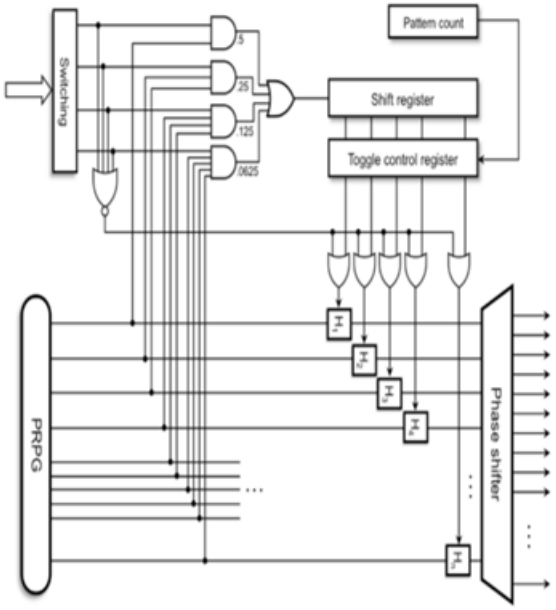


Fig.2 Basic architecture of a PRESTO generator.

The performance of the PRESTO generator depends primarily on the following three factors (note that in the BIST mode they are delivered only once, at the very beginning of the entire test session):
1) The switching code (kept in the switching register);
2) The hold duty cycle (HC);
3) The toggle duty cycle (TC).

The same signal allows the counter to have the input data kept in the Toggle or Hold register entered as the next state. Both the down counter and the T flip-flop [3] need to be initialized every test pattern. The initial value of the T flip flop decides whether the de-compressor will begin to operate either in the toggle or in the hold mode, while the initial value of the counter, further referred to as an offset, determines that mode's duration. As can be seen, functionality of the T flip-flops remains the same as that of the LP PRPG but two cases.

First of all, the encoding procedure may completely disable the hold phase (when all hold latches are blocked) by loading the Hold register with an appropriate code, for example, 0000. If detected (No Hold signal in the figure), it overrides the output of the T flip-flop by using an additional OR gate, as shown in Fig. 8. As a result, the entire test pattern is going to be encoded within the toggle mode exclusively. In addition, all hold latches have to be properly initialized. Hence, a control signal First cycle

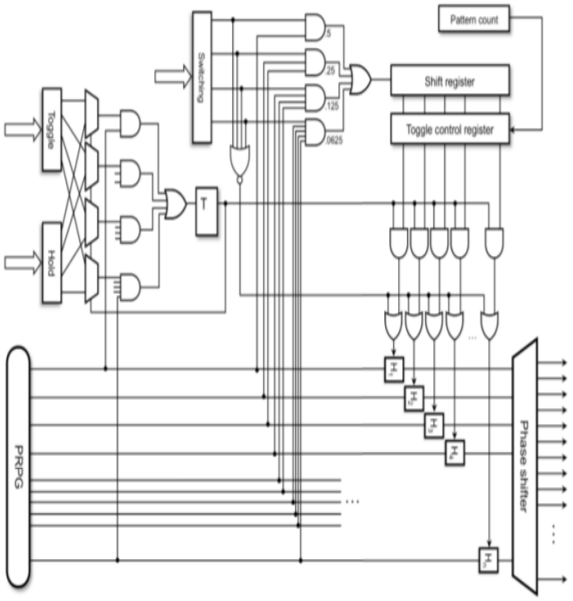
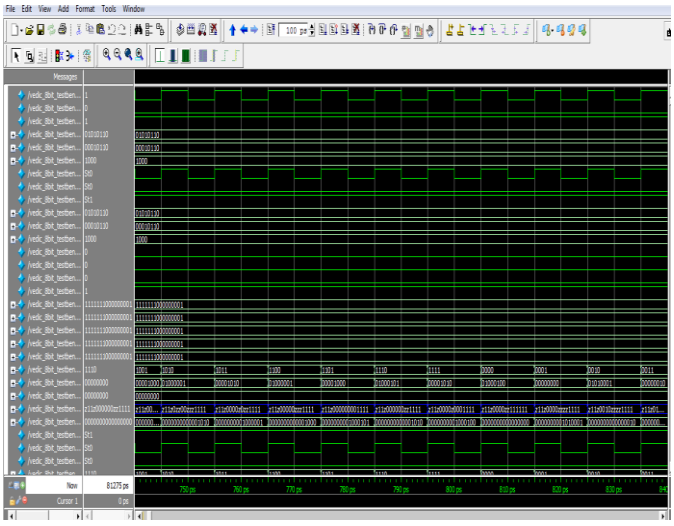


Fig.3 Fully operational version of PRESTO

IV. SOFTWARE IMPLEMENTATION RESULTS

a) Functional verification in Modelsim



b) Performance of area

Flow Summary

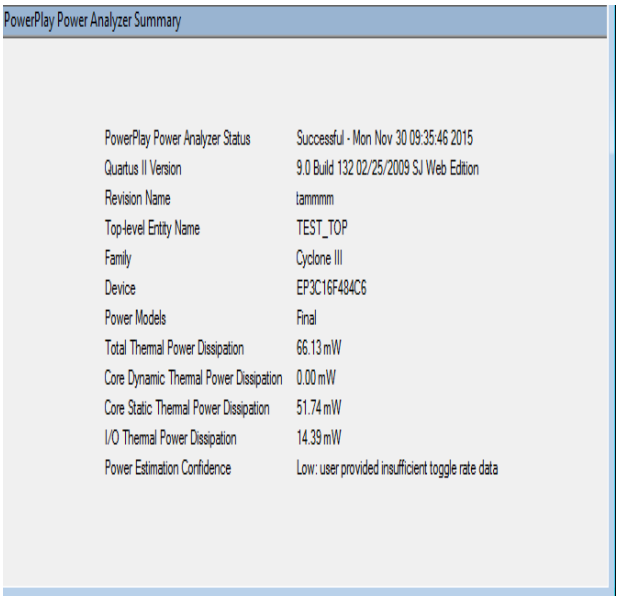
Flow Status	Successful - Mon Nov 30 09:28:46 2015
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	tammmm
Top-level Entity Name	TEST_TOP
Family	Cyclone III
Device	EP3C16F484C6
Timing Models	Final
Met timing requirements	N/A
Total logic elements	413 / 15,408 (3 %)
Total combinational functions	393 / 15,408 (3 %)
Dedicated logic registers	284 / 15,408 (2 %)
Total registers	284
Total pins	23 / 347 (7 %)
Total virtual pins	0
Total memory bits	0 / 516,096 (0 %)
Embedded Multiplier 9-bit elements	0 / 112 (0 %)
Total PLLs	0 / 4 (0 %)

c) Performance of speed

Fmax Summary

	Fmax	Restricted Fmax	Clock Name	Note
1	287.19 MHz	250.0 MHz	clk	limit due to minimum period restriction (max I/O toggle rate)

d) Power analyzer



V. TABLE

TABLE I

Decompressor Type	No. of transitions	Power(mw)
Existing Decompressor	15128	64.76mw
Proposed Decompressor	1003	63.72mw

VI. CONCULSION

In the paper we carried out transition controlled PRNG and the LP decompresser design and its testing quality metrics through modelsim based simulation which can produce pseudorandom test patterns with scan shift-in switching activity precisely. The switching activity can be easily control the generator, so that the resultant test vectors can either yield a desired fault coverage faster than the conventional pseudorandom patterns while still reducing toggling rates down to desired levels, and offer visibly higher coverage numbers if run for comparable test times. And this design is extended into fully functional test data decompressor with the ability to control scan shift-in switching activity through the process of encoding. The efficiency of proposed combine test compression with logic BIST is verified and proved to deliver high quality test.

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